Syntacore™
Custom cores and tools

RISC-V compatible processor IP by Syntacore: compact open-source MCU to octacore SMP Linux

info@syntacore.com

RISC-V Spring Week, Paris
May 2022

Outline

- Company intro
- Current available IPs
- New IP for Q2 release
- SCR 7 benchmarking
- Design environment and tools
- Summary

Syntacore introduction

Semiconductor IP company, founding premier member of RISC-V foundation

Develops and licenses state-of-the-art RISC-V cores

- Immediately available, silicon-proven and ships in volume
- 120+ years of combined RISC-V experience
- 400+ years of relevant background in the team
- SDKs, samples in silicon, full collateral

Full service to specialize CPU IP for customer needs

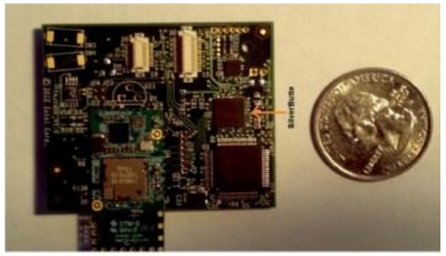
- One-stop workload-specific customization for 10x improvements
  - with tools/compiler support
- IP hardening at the required library node
- SoC integration and SW migration support

Company background

Est 2015 , ~100 EE

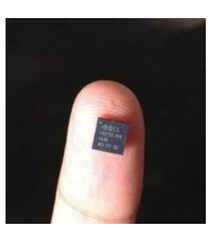
European Headquarters

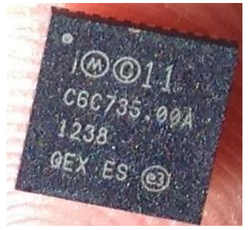
- HQ in Cyprus, UK and APAC business entities
- Full-time staff and representatives in APAC, EMEA and the US



Expertise:

- High-performance and low-power embedded cores and IP
- ASIP technologies and reconfigurable architectures
- Architectural exploration & workload characterization
- Compiler technologies





Focusing on application-class Linux-capable multicore CPU clusters + turnkey customization, in SV

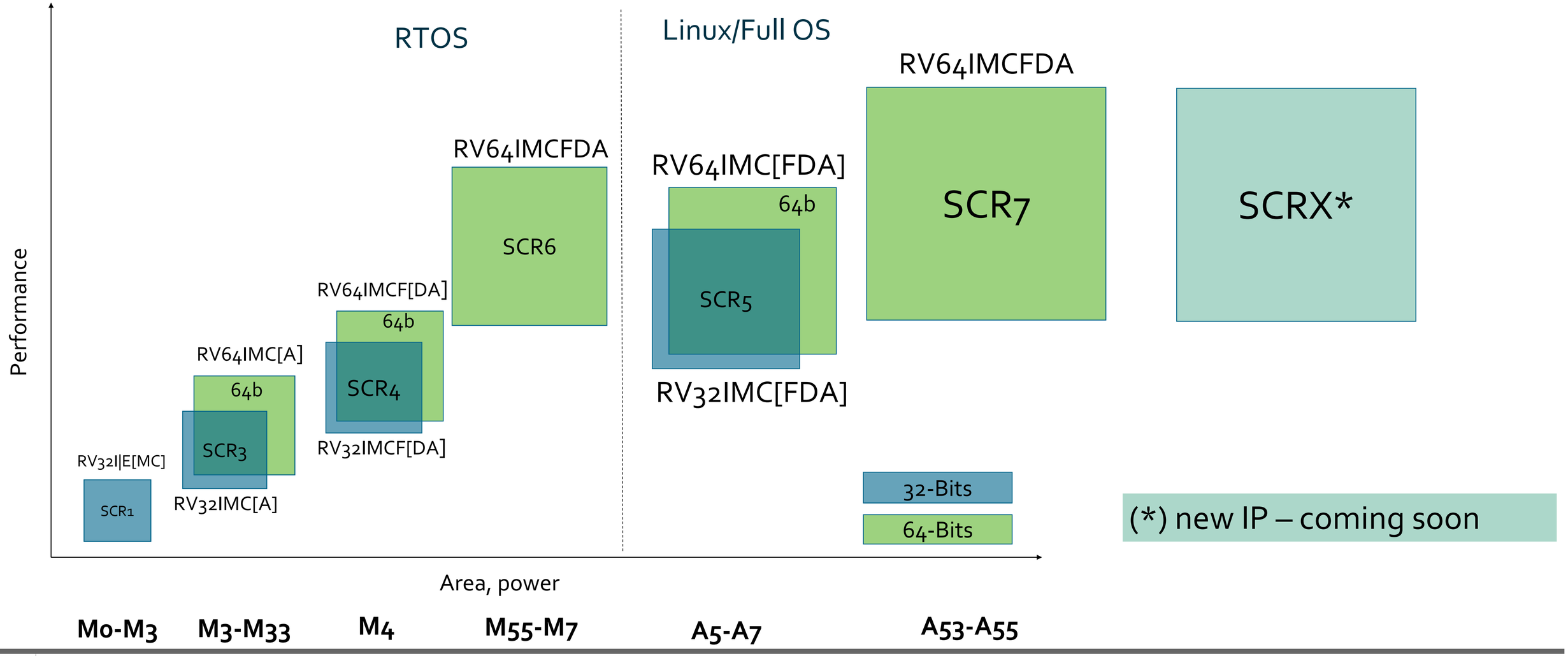
Some current results

- State-of-the-art RISC-V CPU IP line with competitive features
  - ✓ Commercially deployed in SoCs up to 5nm
  - ✓ First RISC-V client silicon in 2016, first RISC-V Linux-capable IP in 2016, in full-wafer from 2017
  - ✓ Projects on 10+ nodes at 5 foundries (230 to 5nm)

- MPWs and full-wafer production. Projects examples:
  - ✓ 56-cores heterogeneous SoC @7nm (64bit, NuMA, complex system arch customization)
  - ✓ Active battery-less SoC @22nm (extensive power optimization, ntv-ready)

- Customers in APAC, EMEA and the US
  - ✓ References available

Current available IPs



(*) new IP – coming soon

Entry-level server-class IP in Q2’22

Linux-capable application-class core, high-level features*:

- 8-16 cores per cluster
- Quad-issue
- Coherent NoC-based L3
- CHI external i/f
- SV39, SV48
- Ztso
- Hypervisor

Pre-announcing today, at lead customers starting Q2’22

(*) some features may be not available in the initial release

State-of-the art RISC-V CPU IP

Features			RTOS/ Bare Metal			Linux/ "Full" OS	
			SCR1* (FREE!)	SCR3	SCR4	SCR5	SCR7
Width	32bit		●	●	●	●	
	64bit			●	●	●	●
ISA			RV32|I|E[MC]	RV32|64IMC[A]	RV32|64IMCF[AD]	RV32|64IMC[AFD]	RV64IMCAFD
Pipeline type			In-order	In-order	In-order	In-order	Superscalar
Pipeline, stages			2-4	3-5	3-5	7-9	10-12
Branch prediction				Static BP, RAS	Static BP, RAS	Static BP, BTB, BHT, RAS	Dynamic BP, BTB, BHT, RAS
Execution priority levels			Machine	User, Machine	User, Machine	User, Supervisor, Machine	User, Supervisor, Machine
Extensibility/customization			●	●	●	●	●
Execution units	MUL/DIV	area-opt	●	O	O	O	
		hi-perf	O	●	●	●	●
	FPU				●	●	● [hi-perf opt]
Memory subsystem	TCM [w/ECC|parity]		●	●	●	●	O
	L1$ [w/ECC|parity]			O	O	●	●
	L2$ [w/ECC]			O	O	O	●
	MPU			●	●	●	●
	MMU, virtual memory					●	●
Debug	Integrated JTAG debug		●	●	●	●	●
	HW BP		1-2	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl
	Performance counters		O	●	●	●	●
Interrupt Controller	IRQs		8-32	8-1024	8-1024	8-1024	8-1024
	Features		basic	advanced	advanced	advanced+	advanced+
SMP support				up to 4 cores with coherency			up to 8-16 cores
I/F options	AHB		●	O	O	O	O
	AXI4		O	●	●	●	●
	ACE						O

* Download SCR1 free at www.github.com/syntacore/scr1

● – default, O – configurable option;
ISA options: I – Integer instruction set; E - Embedded subset (16 registers); M – Integer multiply and divide; A – Atomic memory operations, load-reserve/store conditional; C – Compressed integer instructions, reduces size to 16 bits; F/D – single/double precision (32/64 bit) floating point.

Baseline cores:

- Clean-slate designs in System Verilog
- Configurable and extensible
- 100% compatible with major EDA flows
- Silicon-proven at the customers

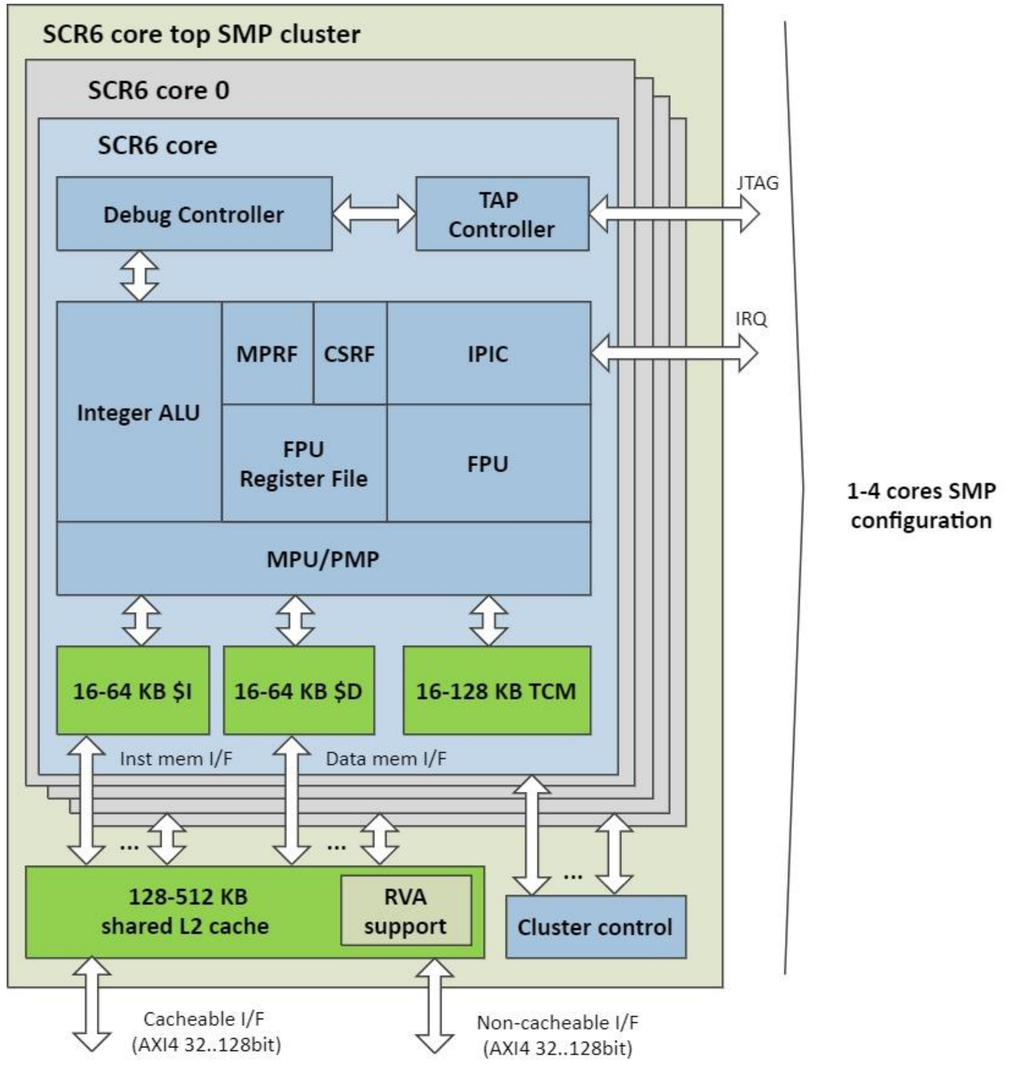
SCR6 (announced at Risc-V summit 2021)

High-perf embedded MCU processor

- RV64IMCAFD ISA
- Dual-issue in-order
- SMP 1-4 cores per cluster
- Dedicated $I/$D up to 64KB each w/ECC
- Per-core or cluster-level TCM
- Shared L2 w/ECC up to 512KB
- Machine and User privilege modes
- Configurable PMP
- Configurable PLIC up to 1023 IRQs
- High-perf dual-issue FPU option
- AMBA compatible i/f
- Advanced debug capabilities

Performance:

- up to 1.5 GHz in 28nm
- 5 CM/MHz/core
- from 500 kGates per core (mem not included)

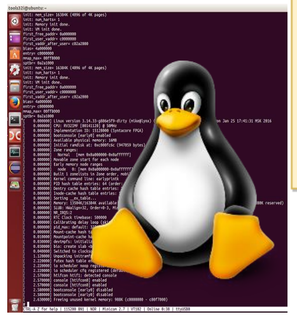


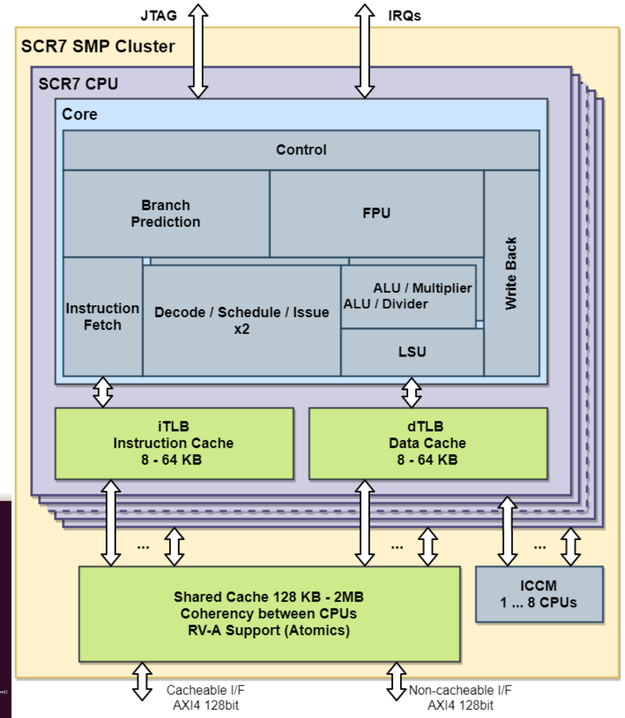
RV64 SCR7

Efficient mid-range application core

- RV64GC ISA
- **SMP up to 8, later 16 cores**
- Flexible uarch template, 10-12 stage pipeline
- Stable SCR7 in production:
  - Decode and dispatch up to two instructions per cycle
  - Out-of-order issue of up to four micro-ops
  - Out-of-order completion, in-order retirement
- M-, S- and U-modes
- Virtual memory support, full MMU, Linux
- 16-64KB L1, up to 2MB L2 cache with ECC
- **1.5 GHz+ @28nm**
- Advanced debug with JTAG i/f

8-core SMP Linux DEMO



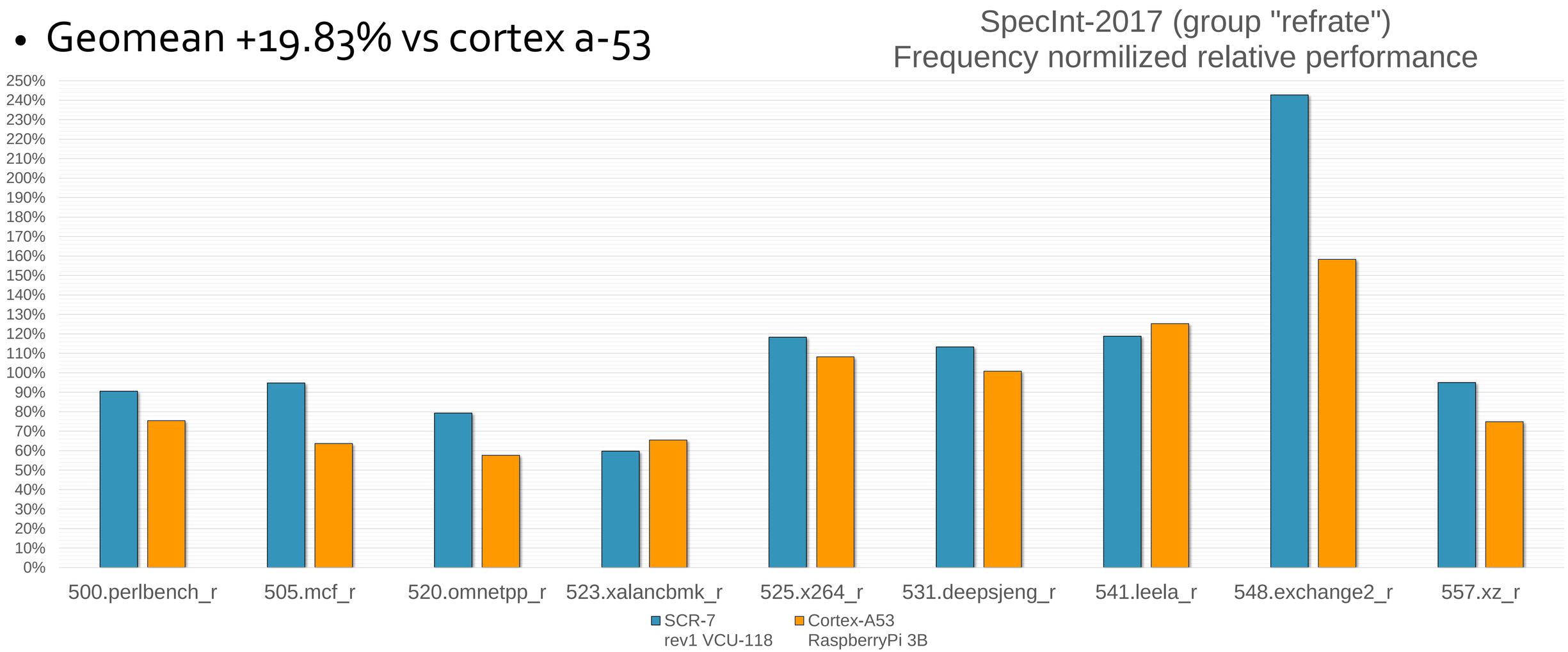


Performance*, per MHz	DMIPS	-O2	3.25
		-best**	3.80
	Coremark	-best**	5.12

* Preliminary data, 2-way implementation, Dhrystone 2.1, Coremark 1.0, GCC 8.1 BM
** O3-funroll-loops -fpeel-loops -fgcse-sm -fgcse-las -flto

SCR7 SpecInt 2017

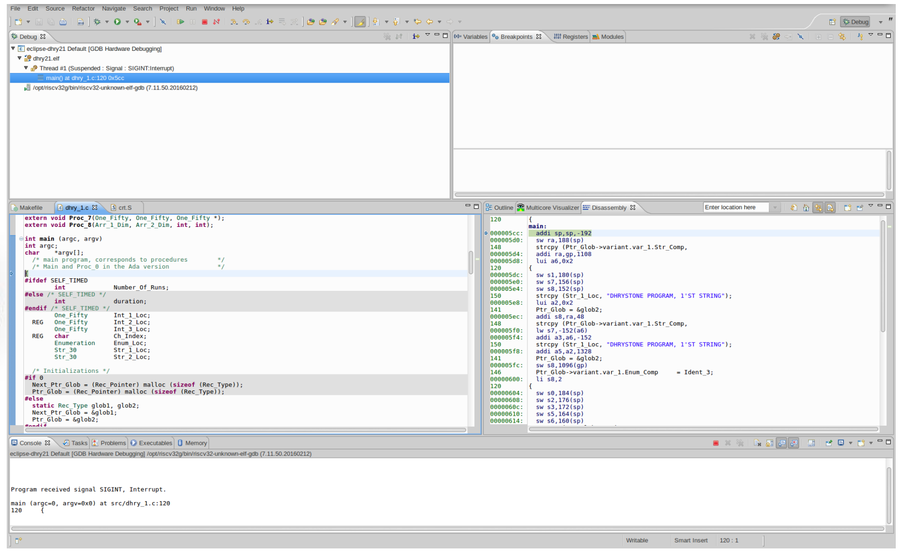
- Geomean +19.83% vs cortex a-53



SCR7 FPGA-based SDK

Fully-integrated system based on the off-the-shelf Xilinx VCU118 dev.kit:
https://www.xilinx.com/products/boards-and-kits/vcu118.html

- Quad-core, 4GB RAM, up to 100-150 MHz, 1GB Ethernet, storage
- Boots upstream Linux kernel 4.19 (5.15 WiP), Debian
- Integrated toolchain with IDE (supports Linux targets debug)
  - Windows: https://yadi.sk/d/S1Ub16jKX2xLwQ
  - Linux: https://yadi.sk/d/8ZsMgUx381GKiw



HTG-960 based (VU19P) dev.kit:
http://www.hitechglobal.com/Boards/VirtexUltraScale+_VU19P_Board.htm

Key benefits of product offering

Application-class Linux-capable multicore CPU clusters + turnkey customization

- Clean-slate, silicon-proven processor IP in System Verilog
  - One of the broadest offerings in the RISC-V ecosystem
- Turnkey service for CPU specialization
  - workload analysis, ISA design, RTL, tools, SW porting
- Experienced team with a proven track record (shipping products)
- Easy evaluation and simplified licensing
- Open-source SCR1 rv32i|e[mc] core with maintenance and support
  - Industry-grade, in full wafer production at the customers

Fully featured SW development suite

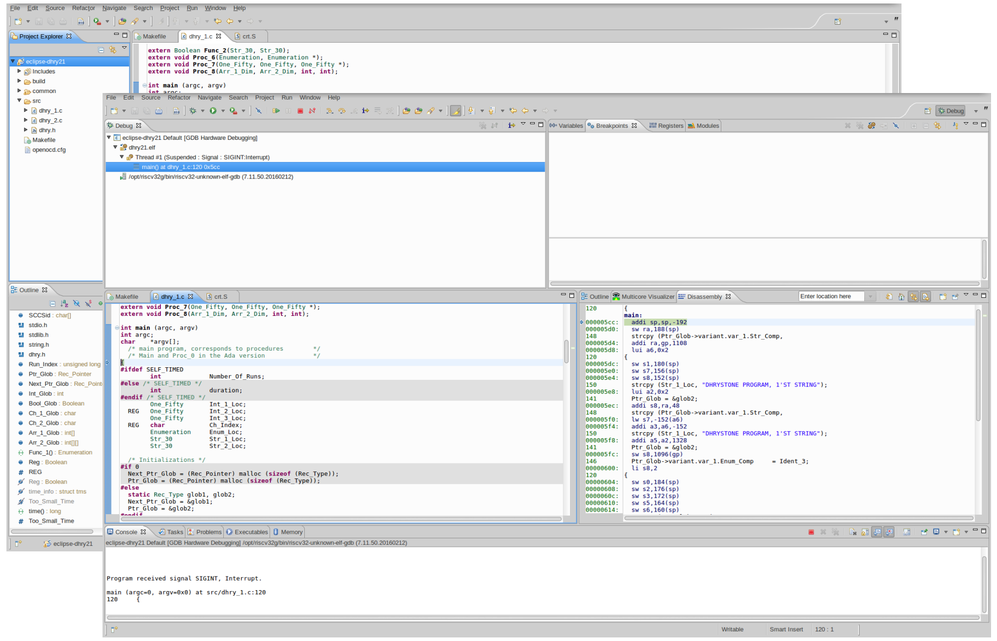
Stable IDE in production:

- GCC 10.2
- GNU Binutils 2.31.0
- Newlib 3.0
- GNU GDB 8.0.50
- Open On-Chip Debugger 0.10.0
- Eclipse 4.9.0

Hosts: Linux, Windows
Targets: BM, Linux

Also available:

- LLVM 5.0
- CompCert 3.1
- 3rd party vendors

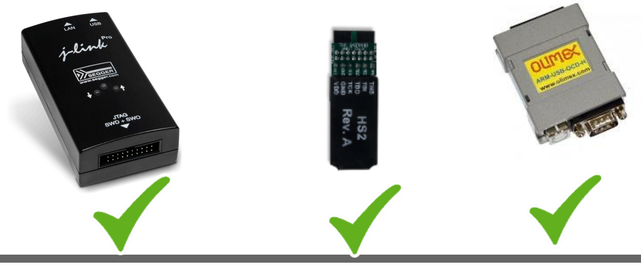


Simulators:

- Qemu
- Spike
- 3rd party vendors

JTAG-based debug solutions:

Supports: Segger J-link, Olimex ARM-USB-OCD family, Digilink JTAG-HS2, more vendors soon



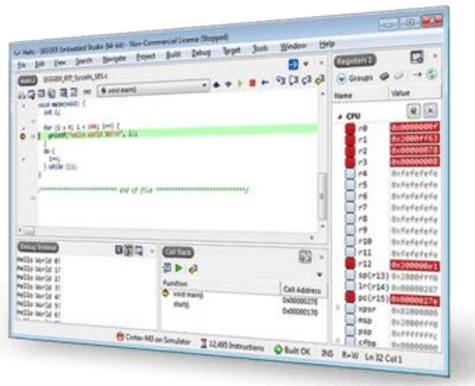
Wide support by 3rd party tools and SW vendors

- Lauterbach Trace32

https://www.lauterbach.com/frames.html?pro/pro__syntacore.html

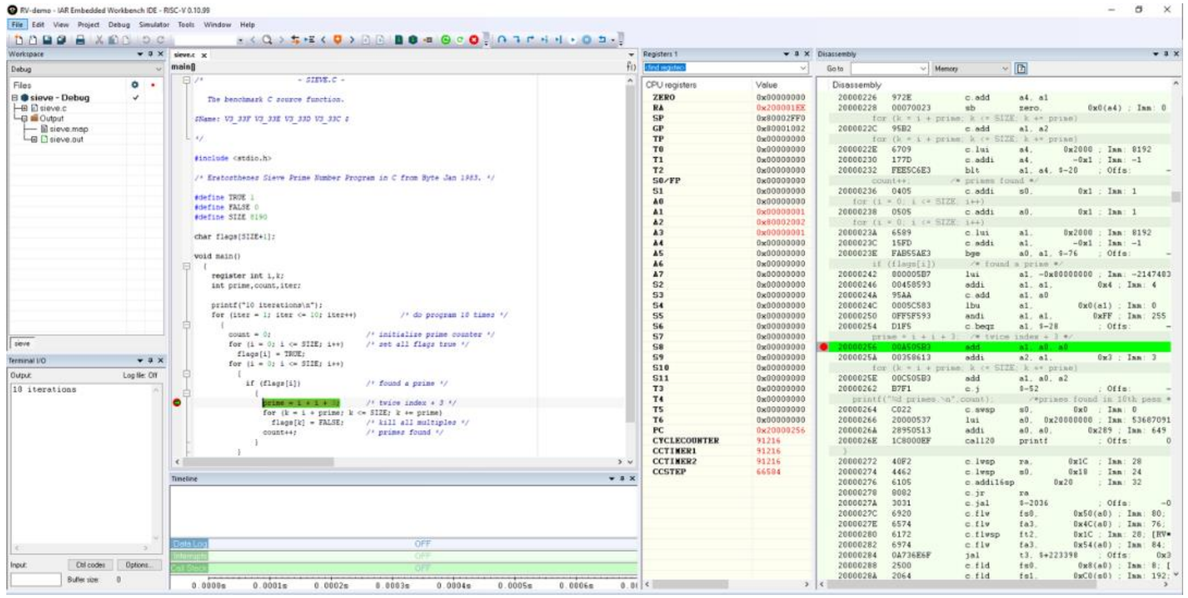
- Segger Embedded Studio

https://wiki.segger.com/Syntacore_SCR1_SDK_Arty



- IAR Embedded Workbench

https://www.iar.com/iar-embedded-workbench/#!?architecture=RISC-V



IP collateral (what is included)

Standard core package (SCR7)

- RISC-V compatible core
  - RV64GC ISA
  - RTL (encrypted for evaluation stage), suitable for simulation and synthesis
  - Netlist for the required FPGA devices (Xilinx/Altera)
- Simulation and verification environment
  - Testbench, Integration verification environment
  - Architectural and compliance tests suites (pre- and post-si)
- Synthesis support harness
  - sample scripts, SDC/timing constraints for the required flow
- Reference instantiation examples
- Back-end support @ required process node (PDK access to be provided)
  - Full cycle: synthesis, floor-planning, netlist verification, PaR/CTS/timing closure, DRC, FEV, DFT)
- Support for 1 tapeout up to a year is included

Tools (pre-built & sources)

- GCC based toolchain
  - complier, debugger, linker, functional simulator, binutils, newlib, openocd
- Eclipse-based IDE (Linux, Windows)

FPGA-based SDK

- Sample FPGA project (open design)
- pre-build FPGA and SW images

SW:

- First stage bootloader (SC-BL)
- Linux for the SDK board, including BSP
- Tests/application samples

Documentation

- SCRx quick-start guide (user manual)
- SCRx EAS (External architecture specification)
- SCRx ISM (Instruction set manual)
- SCRx SDK guide
- Integration verification environment guide
- Tools guide (IDE & CLI)

@extra cost:

- On-site support
- SoC Integration and SW porting
- Hardening

Summary benefits of tools

Key benefits or Syntacore tools and software

- Fully featured open-source development solution with every license
- Choice of 3rd party tools vendors for standard and specialized RISC-V IP
- Open SDK designs
- Extensive collateral and dedicated support

Getting access/evaluation

SCR1

- Is fully open: https://github.com/syntacore/scr1 and https://github.com/syntacore/scr1-sdk
- SHL-licensed with unrestricted commercial use allowed
  - Commercial SLA-based support is available

SCR 3|4|5|6|7

- Full package* access is available after simple evaluation agreement

For more info: evaluation@syntacore.com

(*) sufficient for evaluation and tapeout

Summary

Syntacore offers high-quality RISC-V compatible CPU IP

- Risc-V Founding member, now premium member, fully focused on RISC-V since 2015
- Silicon-proven and shipping in full-wafer production
- Turnkey IP customization services with full tools/compiler support
- Extensive collateral and dedicated support
- Turn-key design upgrade from Legacy solution
- Drop-in socket compatible replacement, including SW stack

Application-class Linux-capable multicore CPU clusters + turnkey customization, in SV

Thank You