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### RISC-V compatible processor IP by Syntacore: compact open-source MCU to octacore SMP Linux

### info@syntacore.com **RISC-V Spring Week, Paris** May 2022







## Outline

- Company intro
- Current available IPs
- New IP for Q2 release
- SCR 7 benchmarking
- Design environment and tools
- Summary





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# Syntacore introduction

Develops and licenses state-of-the-art RISC-V cores

- Immediately available, silicon-proven and ships in volume
- 120+ years of combined RISC-V experience
- 400+ years of relevant background in the team
- SDKs, samples in silicon, full collateral  $\bullet$

#### Full service to specialize CPU IP for customer needs • One-stop workload-specific customization for 10x improvements

- - with tools/compiler support
- IP hardening at the required library node
- SoC integration and SW migration support



- Semiconductor IP company, founding premier member of RISC-V foundation







# Company background

### Est 2015, ~100 EE

European Headquarters

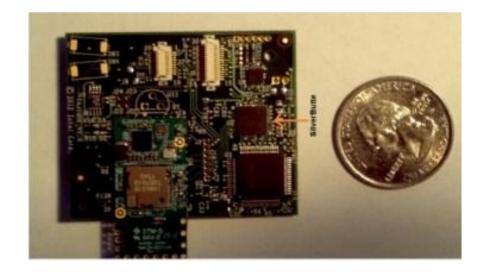
- HQ in Cyprus, UK and APAC business entities
- Full-time staff and representatives in APAC, EMEA and the US

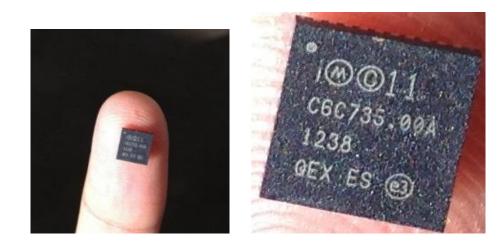
Expertise:

- High-performance and low-power embedded cores and IP
- ASIP technologies and reconfigurable architectures
- Architectural exploration & workload characterization
- Compiler technologies

Focusing on application-class Linux-capable multicore CPU clusters + turnkey customization, in SV











## Some current results

- State-of-the-art RISC-V CPU IP line with competitive features
  - Commercially deployed in SoCs up to 5nm
  - First RISC-V client silicon in 2016, first RISC-V Linux-capable IP in 2016, in full-wafer from 2017
  - Projects on 10+ nodes at 5 foundries (230 to 5nm)
- MPWs and full-wafer production. Projects examples: ✓ 56-cores heterogeneous SoC (@7nm (64bit, NuMA, complex system arch
- customization)
  - $\checkmark$  Active battery-less SoC (a) 22nm (extensive power optimization, ntv-ready)
- Customers in APAC, EMEA and the US References available



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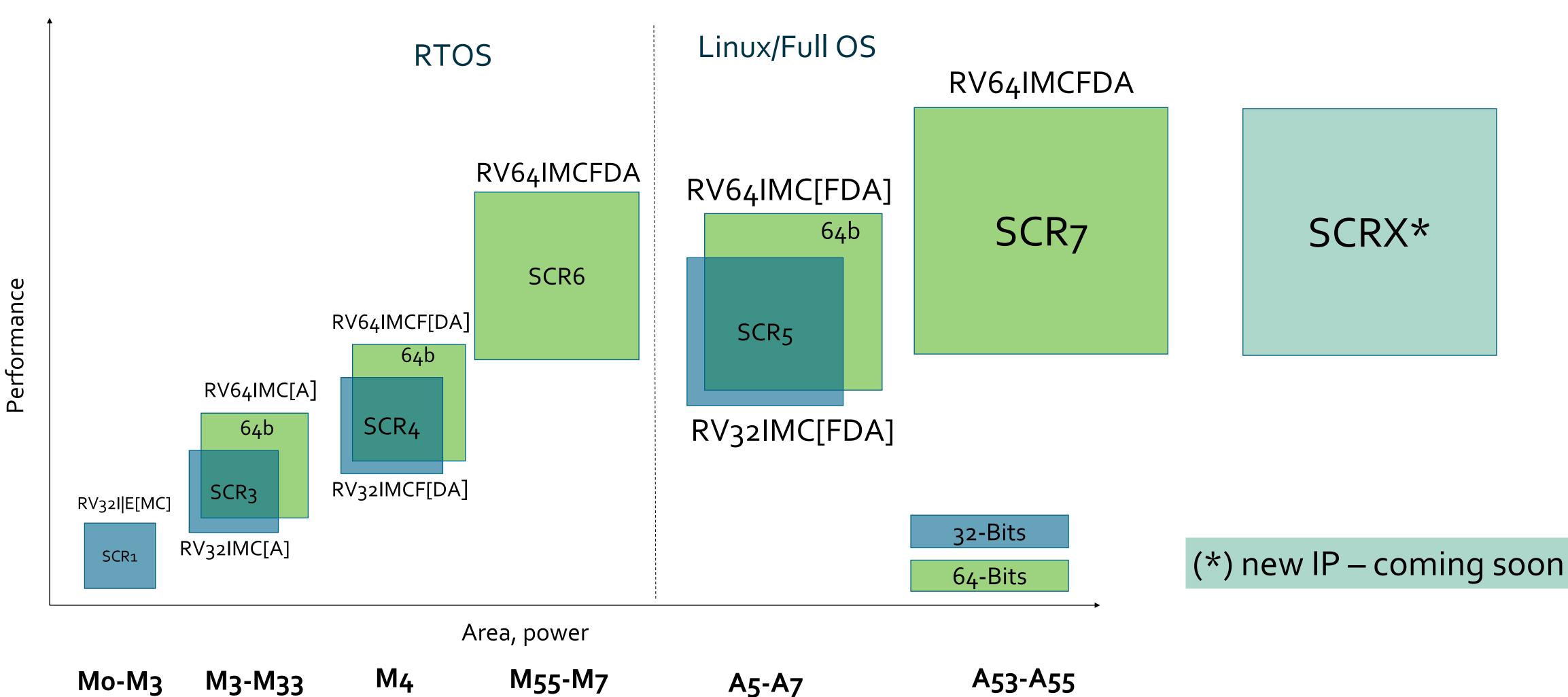






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## Current available IPs





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### Entry-level server-class IP in Q2'22

Linux-capable application-class core, high-level features\*:

- 8-16 cores per cluster
- Quad-issue
- Coherent NoC-based L3
- CHI external i/f
- SV39, SV48
- Ztso
- Hypervisor

Pre-announcing today, at lead customers starting Q2'22

(\*) some features may be not available in the initial release



RISC-V **Sk** 

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### State-of-the art RISC-V CPU IP

eatures		RTOS/ Bare Metal			Linux/ "Full" OS		
		SCR1*	SCR3	SCR4	SCR5	SCR7	
Width	32	bit	۲	•			
64bit			•				
ISA		RV321 E[MC]	RV32 64 MC[A]	RV32 64IMCF[AD]	RV32 64IMC[AFD]	RV64IMCAFD	
Pipeline type			In-order	In-order	In-order	In-order	Superscalar
Pipeline, stages			2-4	3-5	3-5	7-9	10-12
Branch predicti	on			Static BP, RAS	Static BP, RAS	Static BP, BTB, BHT, RAS	Dynamic BP, BTB, BHT, RAS
Execution prior	rity levels		Machine	User, Machine	User, Machine	User, Supervisor, Machine	User, Supervisor, Machine
Extensibility/cus	tomization		•	•			
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UTILS	FP	νU					[hi-perf opt]
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subsystem	L2\$ [w	//ECC]		0	0	0	
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	MMU, virtu	ual memory					
Integrated JTAG debug		•	•				
Debug	HV	N BP	1-2	1-8 ad∨ ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl
	Performan	ce counters	0	•	•		
Interrupt	IR	Qs	8-32	8-1024	8-1024	8-1024	8-1024
Controller	Fea	tures	basic	advanced	advanced	advanced+	advanced+
SMP support				up	to 4 cores with coher	rency	up to 8-16 cores
	AH	HB	•	0	0	0	0
I/F options	A>	<14	0	•	•	•	
	AC	CE					0

 $\bullet$  – default,  $\bullet$  – configurable option;

ISA options: I – Integer instruction set; E - Embedded subset (16 registers); M – Integer multiply and divide; A – Atomic memory operations, load-reserve/store conditional;

C – Compressed integer instructions, reduces size to 16 bits; F/D – single/double precision (32/64 bit) floating point.



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Baseline cores:

- Clean-slate designs in • System Verilog
- Configurable and ulletextensible
- 100% compatible with major EDA flows
- Silicon-proven at the customers











### SCR6 (announced at Risc-V summit 2021)

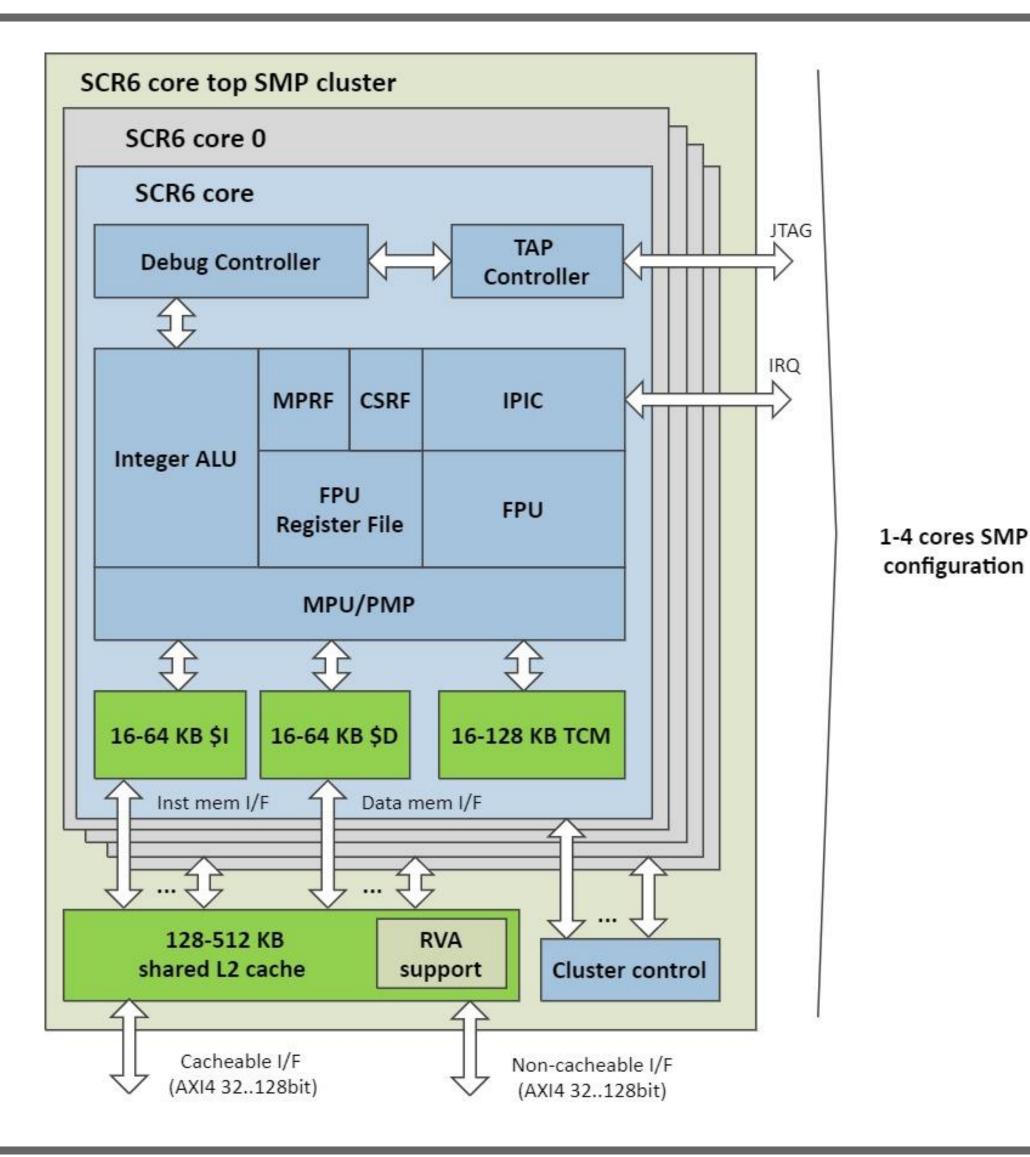
#### High-perf embedded MCU processor

- RV64IMCAFD ISA
- Dual-issue in-order
- SMP 1-4 cores per cluster
- Dedicated \$I/\$D up to 64KB each w/ECC
- Per-core or cluster-level TCM
- Shared L2 w/ECC up to 512KB  $\bullet$
- Machine and User privilege modes  $\bullet$
- Configurable PMP  $\bullet$
- Configurable PLIC up to 1023 IRQs  $\bullet$
- High-perf dual-issue FPU option
- AMBA compatible i/f
- Advanced debug capabilities

Performance:

- up to 1.5 GHz in 28nm
- 5 CM/MHz/core
- from 500 kGates per core (mem not included)





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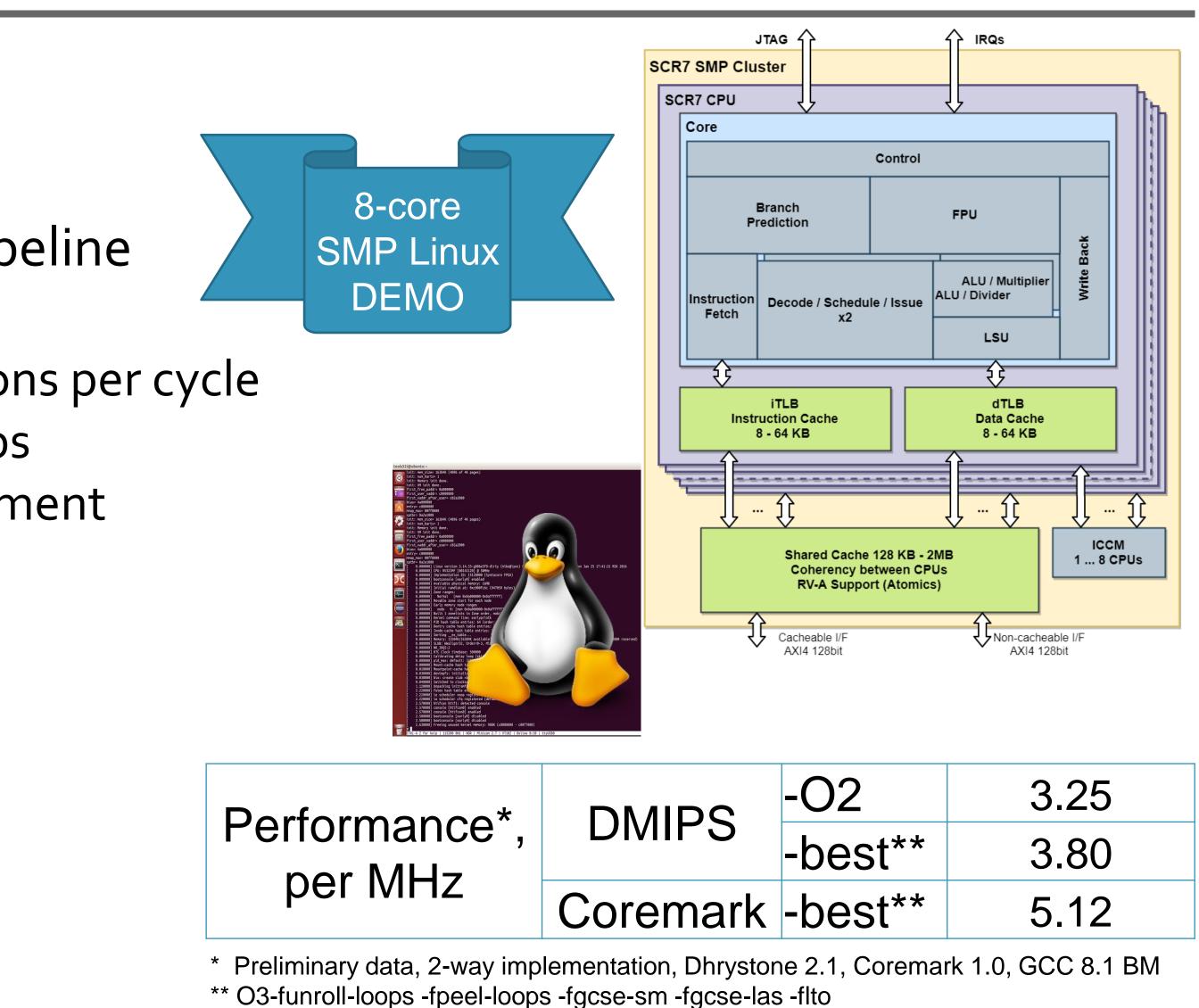


## RV64 SCR7

### **Efficient mid-range application core**

- RV64GC ISA
- SMP up to 8, later 16 cores
- Flexible uarch template, 10-12 stage pipeline
- Stable SCR7 in production:
  - Decode and dispatch up to two instructions per cycle
  - Out-of-order issue of up to four micro-ops
  - Out-of-order completion, in-order retirement
- M-, S- and U-modes
- Virtual memory support, full MMU, Linux
- 16-64KB L1, up to 2MB L2 cache with ECC
- 1.5 GHz+ @28nm
- Advanced debug with JTAG i/f





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## SCR7 SpecInt 2017

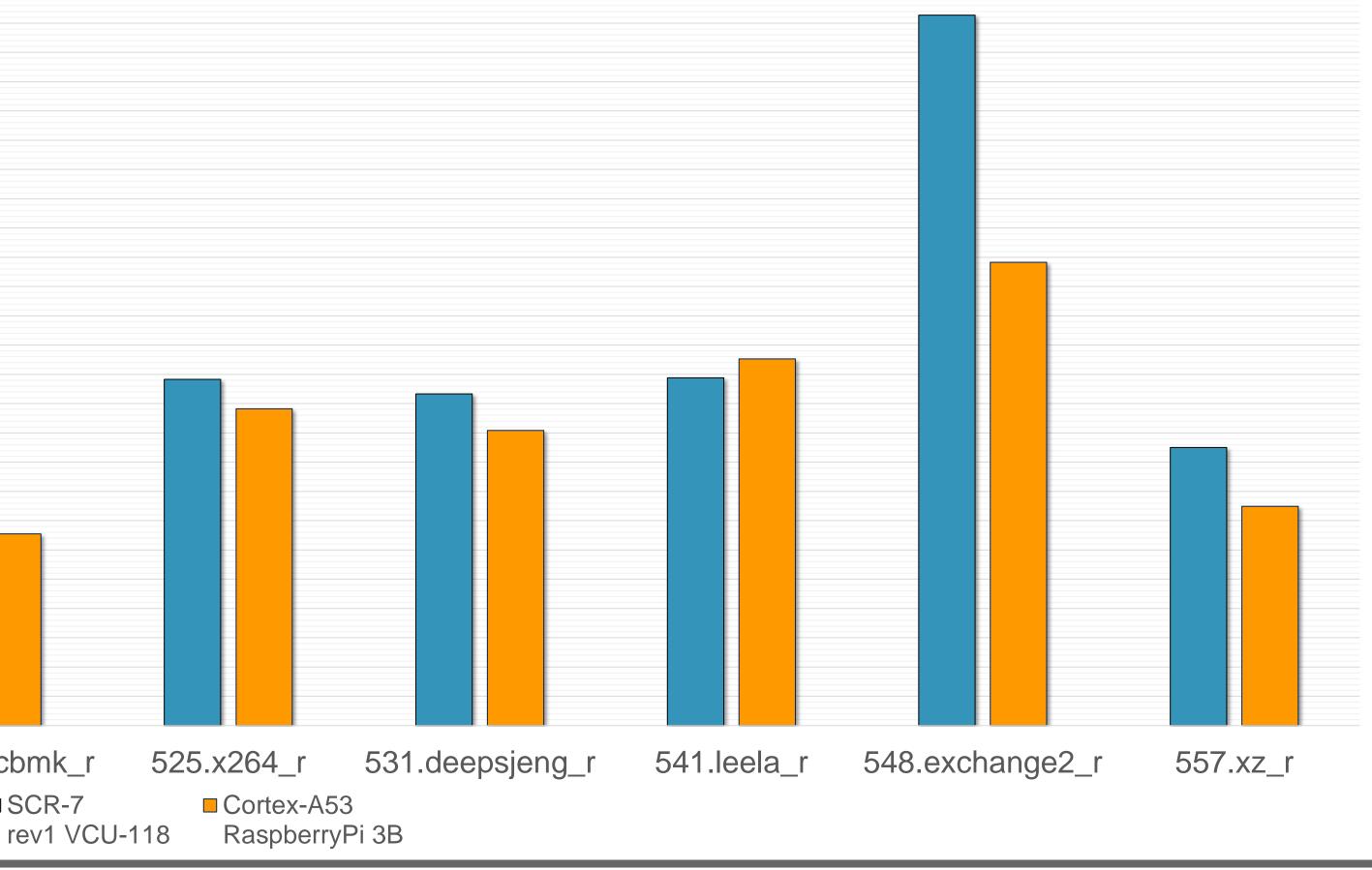
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				■ SCR-7
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#### SpecInt-2017 (group "refrate") Frequency normilized relative performance



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RISC-V

## SCR7 FPGA-based SDK

Fully-integrated system based on the off-the-shelf Xilinx VCU118 dev.kit: https://www.xilinx.com/products/boards-and-kits/vcu118.html

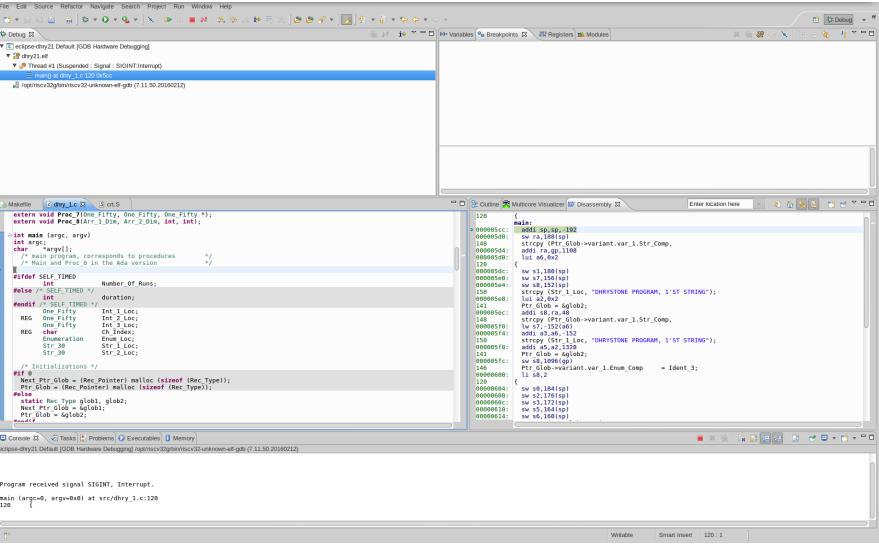
- Quad-core, 4GB RAM, up to 100-150 MHz, 1GB Ethernet, storage
- Boots upstream Linux kernel 4.19 (5.15 WiP), Debian
- Integrated toolchain with IDE (supports Linux targets debug)
  - Windows: <u>https://yadi.sk/d/S1Ub16jKX2xLwQ</u>
  - Linux: <u>https://yadi.sk/d/8ZsMqUx381GKiw</u>

### HTG-960 based (VU19P) dev.kit:

http://www.hitechglobal.com/Boards/VirtexUltraScale+\_VU19P\_Board.htm







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### Key benefits of product offering

# Application-class Linux-capable multicore CPU clusters + turnkey customization

- Clean-slate, silicon-proven processor IP in System Verilog
  - One of the broadest offerings in the RISC-V ecosystem
- Turnkey service for CPU specialization
  - workload analysis, ISA design, RTL, tools, SW porting
- Experienced team with a proven track record (shipping products)
- Easy evaluation and simplified licensing
- Open-source SCR1 rv32i[e[mc] core with maintenance and support
  - Industry-grade, in full wafer production at the customers







### Fully featured SW development suite

### Stable IDE in production:

- GCC 10.2
- GNU Binutils 2.31.0
- Newlib 3.0
- GNU GDB 8.0.50
- Open On-Chip Debugger 0.10.0
- Eclipse 4.9.0

#### Hosts: Linux, Windows Targets: BM, Linux

#### Also available:

- LLVM 5.0
- CompCert 3.1
- 3<sup>rd</sup> party vendors



#### Simulators:

- Qemu
- Spike
- 3<sup>rd</sup> party
   vendors

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JTAG-based debug solutions:

Supports: Segger J-link, Olimex ARM-USB-OCD family, Digilink JTAG-HS2, more vendors soon



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### Wide support by 3<sup>rd</sup> party tools and SW vendors

• Lauterbach Trace32

https://www.lauterbach.com/frames.html?pro/pro\_\_syntacore.html

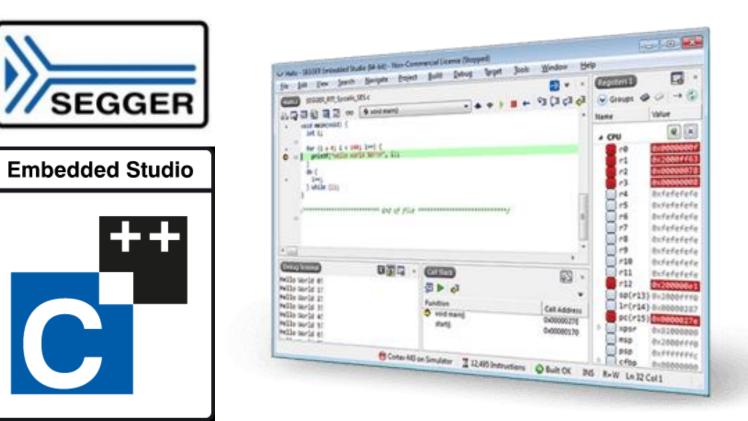


TRACE 32°

r for RISC-

### Segger Embedded Studio

https://wiki.segger.com/Syntacore\_SCR1\_SDK\_Arty









### IAR Embedded Workbench

https://www.iar.com/iar-embedded-workbench/#!?architecture=RISC-V



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		register int i.kr		A7	0x00000000	20000242	800005B7	lui	al0x80	000000
		int prime, count, iter;		52	0x00000000	20000246	00458593	addi	al. al.	987252
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		printf("10 iterations\s");		54	0x00000000	2000024C	0005C583	1bu	a1.	0x0
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## IP collateral (what is included)

#### Standard core package (SCR7)

- RISC-V compatible core
  - RV64GC ISA
  - RTL (encrypted for evaluation stage), suitable for simulation and synthesis
  - Netlist for the required FPGA devices (Xilinx/Altera)
- Simulation and verification environment
  - Testbench, Integration verification environment
  - Architectural and compliance tests suites (pre- and post-si)
- Synthesis support harness
  - sample scripts, SDC/timing constraints for the required flow
- Reference instantiation examples
- Back-end support @ required process node (PDK access to be provided)
  - Full cycle: synthesis, floor-planning, netlist verification, PaR/CTS/timing closure, DRC, FEV, DFT)
- Support for 1 tapeout up to a year is included

#### Tools (pre-built & sources)

- GCC based toolchain
  - complier, debugger, linker, functional simulator, binutils, newlib, openocd
- Eclipse-based IDE (Linux, Windows)



#### FPGA-based SDK

- Sample FPGA project (open design)
- pre-build FPGA and SW images

#### SW:

- First stage bootloader (SC-BL)
- Linux for the SDK board, including BSP
- Tests/application samples

#### Documentation

- SCRx quick-start guide (user manual)
- SCRx EAS (External architecture specification)
- SCRx ISM (Instruction set manual)
- SCRx SDK guide
  - Integration verification environment guide
  - Tools guide (IDE & CLI)

#### @extra cost:

- On-site support
- SoC Integration and SW porting
- Hardening





### Summary benefits of tools

Key benefits or Syntacore tools and software

- Fully featured open-source development solution with every license
- Choice of 3<sup>rd</sup> party tools vendors for standard and specialized RISC-V IP
- Open SDK designs
- Extensive collateral and dedicated support









### Getting access/evaluation

### SCR1

- Is fully open: <u>https://github.com/syntacore/scr1</u> and https://github.com/syntacore/scr1-sdk
- SHL-licensed with unrestricted commercial use allowed Commercial SLA-based support is available

### SCR 3|4|5|6|7

• Full package\* access is available after simple evaluation agreement

### For more info: <a href="mailto:evaluation@syntacore.com">evaluation@syntacore.com</a>

#### (\*) sufficient for evaluation and tapeout









### Summary

Syntacore offers high-quality RISC-V compatible CPU IP Risc-V Founding member, now premium member, fully focused

- on RISC-V since 2015
- Silicon-proven and shipping in full-wafer production
- Extensive collateral and dedicated support
- Turn-key design upgrade from Legacy solution
- Drop-in socket compatible replacement, including SW stack customization, in SV



 Turnkey IP customization services with full tools/compiler support Application-class Linux-capable multicore CPU clusters + turnkey





# Thank You







