

From Technology to Product

Maturing the **RISC-V** Ecosystem



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Rich RISC-V Ecosystem Available Today

HPC Consumer Data Center IoT Networking

Training Academia Research

CI/Testing Buildbot

Perf Tools Sparta gprof

Simulators SAIL QEMU

Compilers SPIKE GCC LLVM

Applications SSH, Open vSwitch, ceph, Apache

Infrastructure docker, redis, MySQL

Runtimes Python, PHP, OpenJDK, SPDK, DDPK, OpenSSL

Operating Systems android, seL4, FreeBSD, Zephyr, RTOS, debian

Hypervisor KVM

Boot OpenSBI, U-Boot

SAIL Golden Model **RISC-V ISA** **Architecture Tests** RISC-V COMPATIBLE

RTL DV

Implementation Design & Microarchitecture

OPENHW ALLIANCE CHIPS ALLIANCE lowRISC

Silicon Soft IP

Reliable, Serviceable, Diagnosable

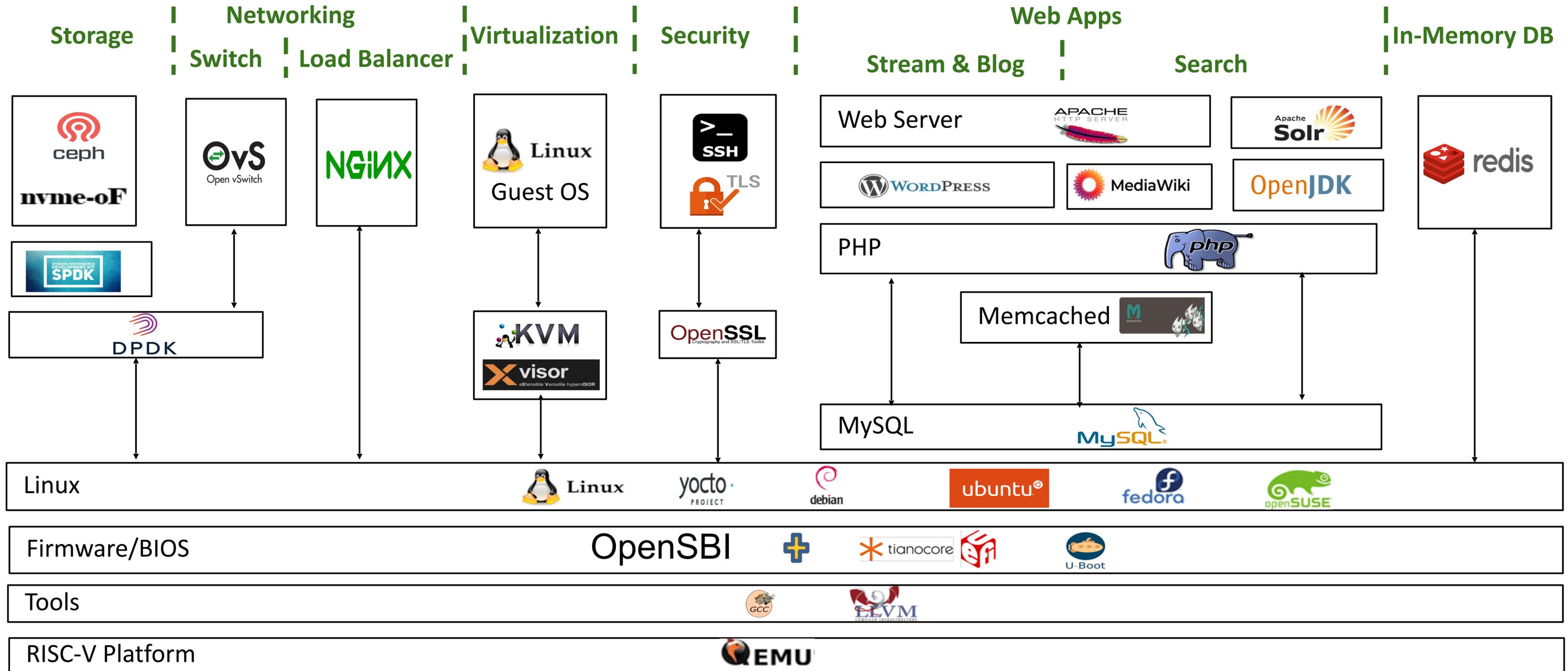
Performant

Secure

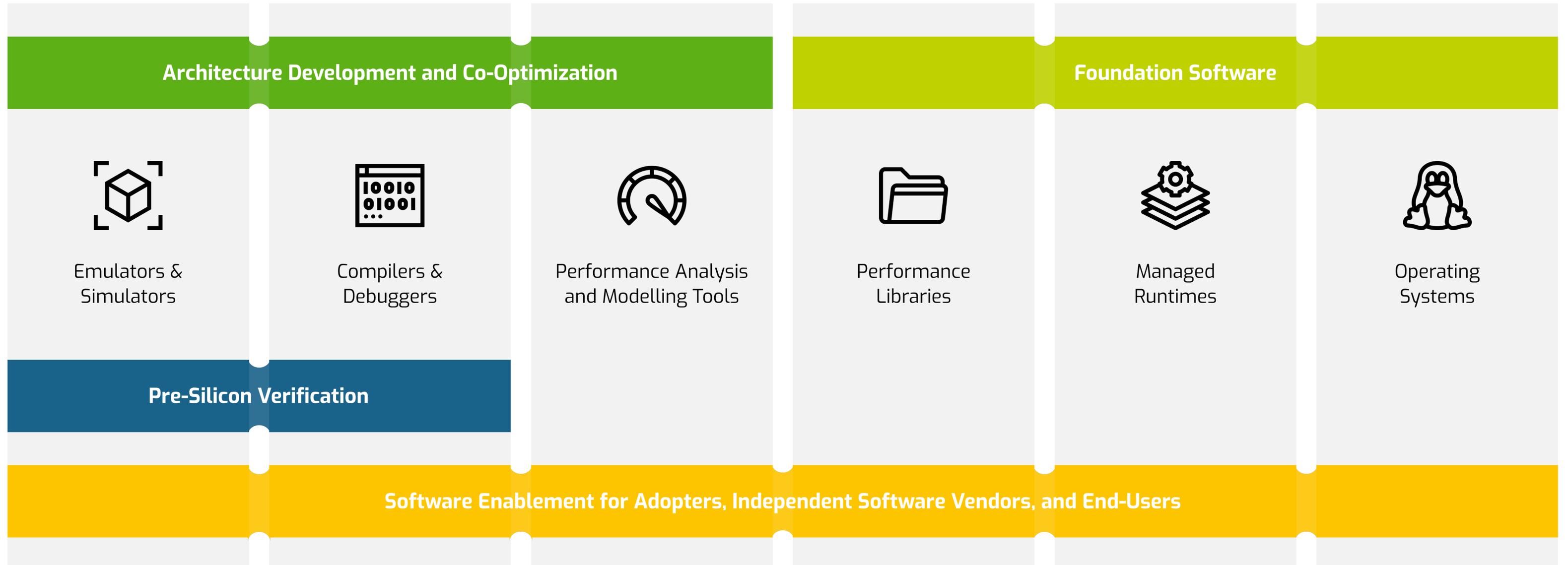
Debugable

Services

Software Stack Examples



Addressing stakeholder needs in the ecosystem



The three principles of the RISC-V ecosystem



Simplified workflow for end-to-end performance



Performance Modelling

Collaboratively built easy-to-use performance modelling framework for RISC-V

SPARTA
modelling
framework



Performance Analysis

Performance monitoring built into the architecture and enabled by the best-in-class analysis tools



Optimised code-speed

Cross-vendor collaboration provides optimised open source compilers and runtimes



Modularity + Customisation = Innovation

Modular ISA



Vendor-defined (custom) ISA extensions

Created policies for naming of custom instructions to support **coexistence** across common open-source tools.

Tools and simulators

Community-adopted policies for including **publicly documented** vendor-defined extensions in key open-source tools.

RISC-V Profiles will enhance the usability.



Dynamic discovery

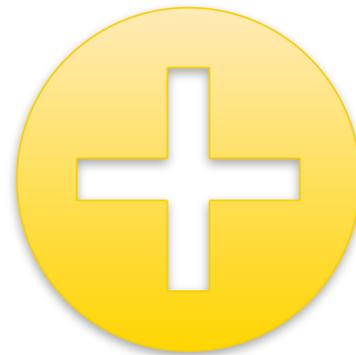
Multiple mechanisms to select **optimised code paths** are fully implemented in libraries and the Linux kernel

Optimised cache management, cryptography, and string functions are **just the beginning**.



OpenJDK19 will natively support RISC-V

RISC-V compiler support merged on March 24th, 2022



<https://github.com/openjdk/jdk/commit/5905b02c0e2643ae8d097562f181953f6c88fc89>

Android 12 running on RISC-V with optimised AI performance

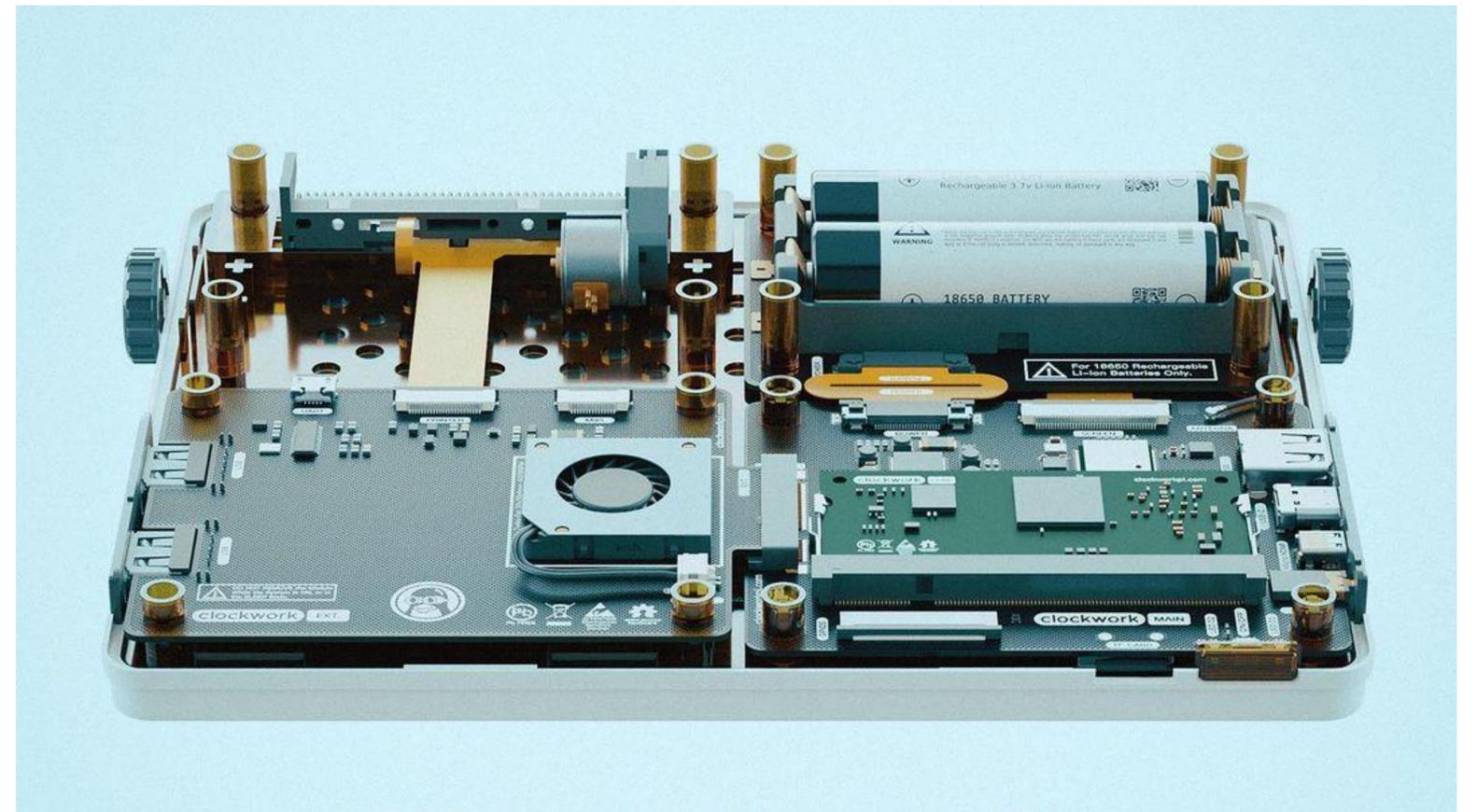


<https://chipsalliance.org/announcement/2022/04/21/alibaba-cloud-announced-progress-in-porting-android-functions-onto-risc-v/>

<https://www.techradar.com/news/alibaba-cloud-is-close-to-getting-android-working-on-risc-v-silicon>

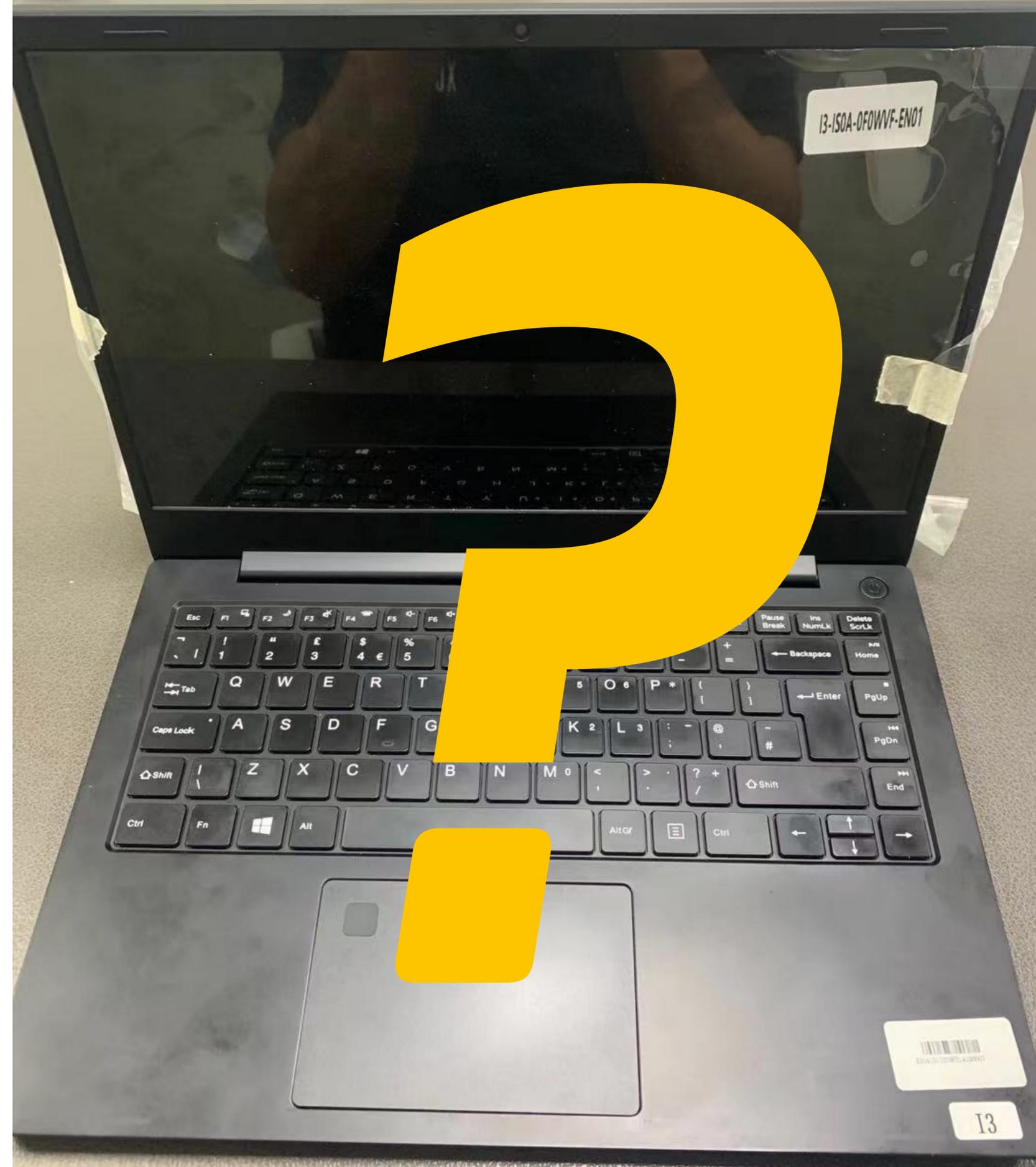
ClockworkPI announced the DevTerm R-01

A turnkey development kit for educators and hobbyists



<https://www.hackster.io/news/clockwork-pi-launches-highly-experimental-risc-v-variant-of-its-compact-devterm-portable-pc-021ad546e675>

**Will we see the
first RISC-V laptop
released in 2022?**



Thank you!

 <https://lists.riscv.org/g/software>

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