THALES
Building a future we can all trust

An Open-Source Application Core:CVA6 from the OpenHW Group

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www.thalesgroup.com

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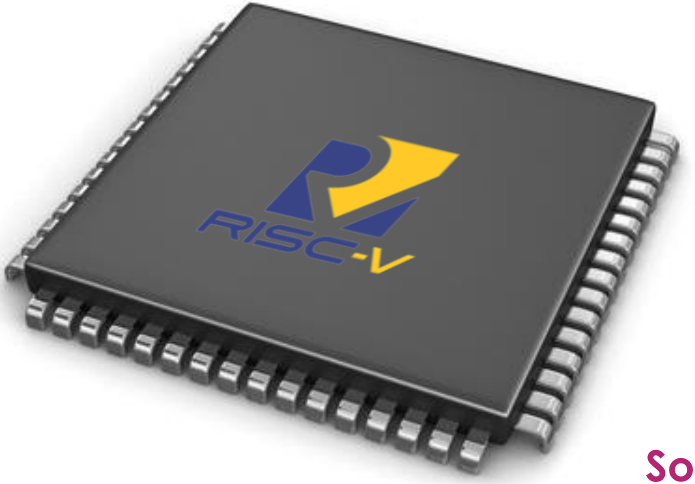
Why Thales invests in RISC-V and open-source HW

Software
Large ecosystem compatible across implementations

Security
A fully auditable processor

Safety
No black-box



SWaP & customization
Exact fit between features and application needs

Performance
State-of-the-art processor

No vendor-locking
LTS; business opportunities for support, customization…

Sovereignty
Ability to fork if needed

Thales member of OpenHW Group and RISC-V International

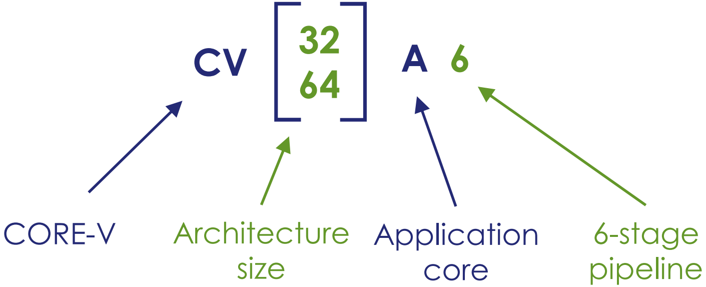
CVA6 core

Open-source RISC-V application core

- Supports rich OSes like Linux

One RTL code base, two flavors:

- **CV64A6**
  - 64-bit
  - ARIANE donated to OpenHW Group by ETH Zürich
- **CV32A6**
  - 32-bit
  - Compact version designed by Thales



CVA6 in a nutshell

Configurable CPU core:
- 32 or 64 bit RISC-V (CV32A6 / CV64A6)
- L1 cache organization
- SP/DP floating point
- Instruction set extension interface (CV-X-IF)
- MMU
- Memory protection (PMP)
- Hypervisor support (H)
- Safe & secure features

Same core
- For **ASIC targets** (32/64 bit)
- As a 32-bit vendor-independent **FPGA soft-core**

Software support:
- Linux (32/64 bit)
- Embedded OS (FreeRTOS…)
- RISC-V standard compilers (GCC…)
- Debug: GDB, OpenOCD, Eclipse IDE

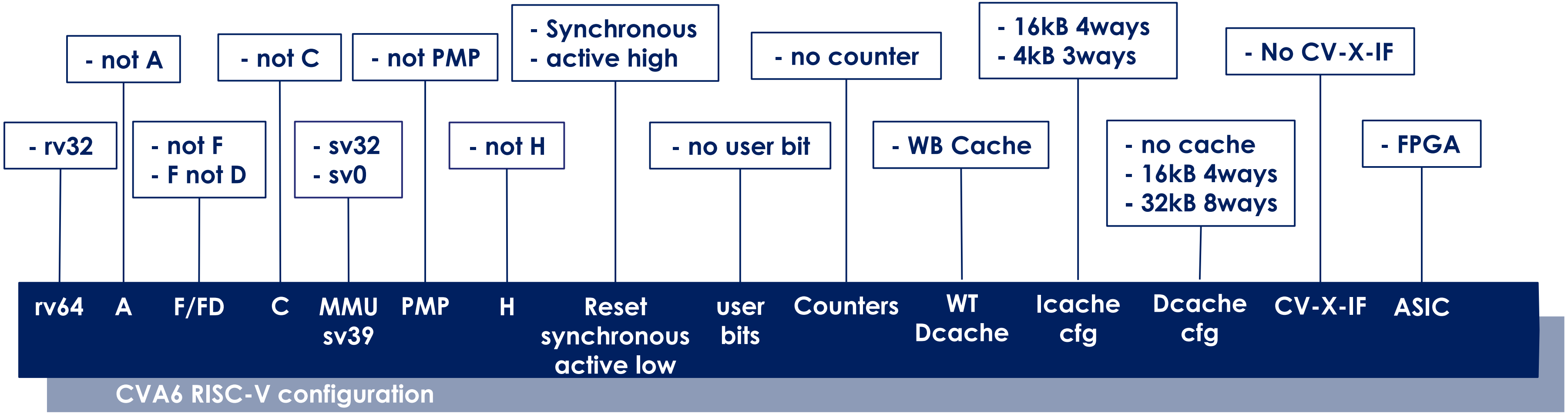
An academic project turning into an **industrial-grade** CPU core
- 100% coverage verification target
- Permissive Apache/Solderpad license

Architecture:
6-stage, single-issue, in-order, branch prediction, 2.5 CoreMark/MHz
CVA6 can be assembled into a **multi/many-core SMP CPU** with OpenPiton
CV32A6: RV32IMA[F][C]_Zicsr_Zifencei M/S/U [Sv32]
CV64A6: RV64IMA[F[D]][C]_Zicsr_Zifencei M/S/U[/H] [Sv39]

[ ] optional feature

Requirement specification:
https://github.com/openhwgroup/cva6/blob/master/docs/specifications/cva6_requirement_specification.rst

CVA6: a highly configurable core



- rv64: - rv32
- A: - not A
- F/FD: - not F, - F not D
- C: - not C
- MMU sv39: - sv32, - sv0
- PMP: - not PMP
- H: - not H
- Reset synchronous active low: - Synchronous, - active high
- user bits: - no user bit
- Counters: - no counter
- WT Dcache: - WB Cache
- Icache cfg: - 16kB 4ways, - 4kB 3ways
- Dcache cfg: - no cache, - 16kB 4ways, - 32kB 8ways
- CV-X-IF: - No CV-X-IF
- ASIC: - FPGA

CVA6 RISC-V configuration

CVA6: an extendable core

CV-X-IF interface to extend the CVA6 instruction set

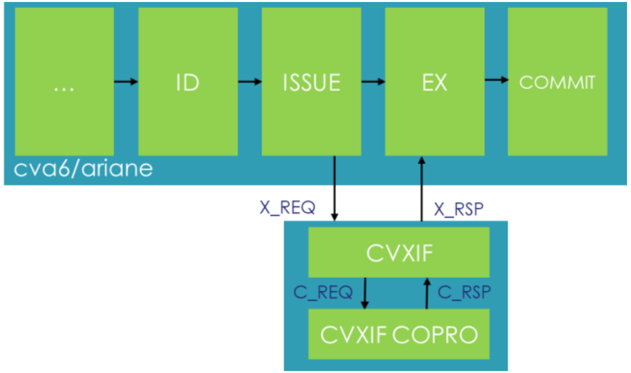
- Current or future RISC-V extensions (B, P…)
- Custom extensions (cryptography, signal processing…)

CV-X-IF specified by OpenHW Group

- Open specification, can be used off OpenHW

Compiler support

- Seamless for supported standard extensions (e.g. B)
- LLVM should ease the support of custom extensions
- Inline ASM possible for specific processing



Benefits

- Add extensions without a full re-validation of the core
- Reuse coprocessors between CORE-V cores (CVA6, CV32E40X, CVE2 tbc)

Building a future we can all trust

FPGA soft-core

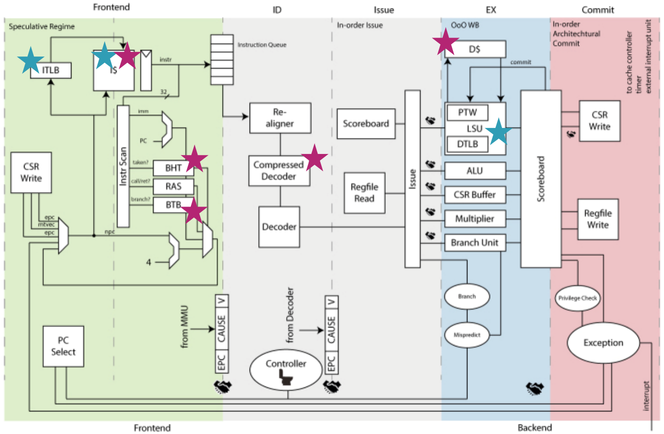
CVA6 initially designed for ASIC targets

CV32A6 is being optimized to also be an FPGA soft-core

- Technology-agnostic (Xilinx, Microchip…)
- Same common RTL code
- Benefits: ease FPGA technology migration, same architectures in ASIC & FPGA, white box analysis…

FPGA optimizations:

- +50% frequency achieved ★
- -30% resources achieved ★
- **More optimizations to come**
- Some also improve ASIC PPA and CV64A6



Linux support and toolchain

MMU

- I&D TLB, hardware PTW
- Designed Sv32 MMU (CV32A6) to complement Sv39 (CV64A6)

Linux support

- Available in 32 & 64 bit
- Currently supported: U-Boot, OpenSBI, BuildRoot
- Yocto to come

Other OSes

- FreeRTOS 32 & 64 bit supported
- As an application core, it should support many other OSes

Compiler: GCC

- CVA6 features RISC-V standard extensions
- LLVM and custom extension support on the roadmap roadmap

Debug: GDB, OpenOCD, Eclipse IDE

Have you visited our demo on OPENHW GROUP booth ?

Open-source project

Full open-source package

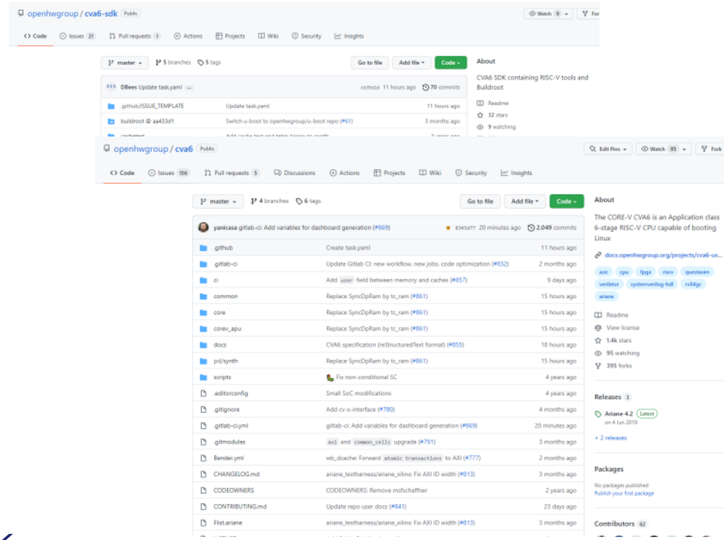
- CVA6 core
- Verification: testbench, sequences, ISS…
- Linux support

Benefits

- Easier collaboration
- Evaluate CVA6 without paperwork
- Audit and white box analysis (safety, security)
- Apache/Solderpad permissive license eases industrial use

Repos

- Core: https://github.com/openhwgroup/cva6
- Linux: https://github.com/openhwgroup/cva6-sdk
- Verification: https://github.com/openhwgroup/core-v-verif



openhwgroup / cva6-sdk

5 branches 5 tags

DBees Update task.yaml … ca35e8a 11 hours ago 70 commits

.github/ISSUE_TEMPLATE	Update task.yaml	11 hours ago
buildroot @ aa433d1	Switch u-boot to openhwgroup/u-boot repo (#61)	3 months ago

About

CVA6 SDK containing RISC-V tools and Buildroot

Readme
32 stars
9 watching

openhwgroup / cva6

4 branches 6 tags

yanicasa gitlab-ci: Add variables for dashboard generation (#869) 8343d77 20 minutes ago 2,049 commits

.github	Create task.yaml	11 hours ago
.gitlab-ci	Update Gitlab CI: new workflow, new jobs, code optimization (#832)	2 months ago
ci	Add `user` field between memory and caches (#857)	9 days ago
common	Replace SyncDpRam by tc_ram (#861)	15 hours ago
core	Replace SyncDpRam by tc_ram (#861)	15 hours ago
corev_apu	Replace SyncDpRam by tc_ram (#861)	15 hours ago
docs	CVA6 specification (reStructuredText format) (#855)	18 hours ago
pd/synth	Replace SyncDpRam by tc_ram (#861)	15 hours ago
scripts	Fix non-conditional SC	4 years ago
.editorconfig	Small SoC modifications	4 years ago
.gitignore	Add cv-x-interface (#780)	4 months ago
.gitlab-ci.yml	gitlab-ci: Add variables for dashboard generation (#869)	20 minutes ago
.gitmodules	`axi` and `common_cells` upgrade (#791)	3 months ago
Bender.yml	wb_dcache: Forward `atomic transactions` to AXI (#777)	2 months ago
CHANGELOG.md	ariane_testharness/ariane_xilinx: Fix AXI ID width (#813)	3 months ago
CODEOWNERS	CODEOWNERS: Remove msfschaffner	2 years ago
CONTRIBUTING.md	Update repo user docs (#841)	23 days ago
Flist.ariane	ariane_testharness/ariane_xilinx: Fix AXI ID width (#813)	3 months ago

About

The CORE-V CVA6 is an Application class 6-stage RISC-V CPU capable of booting Linux

docs.openhwgroup.org/projects/cva6-us...

asic cpu fpga riscv questasim verilator systemverilog-hdl rv64gc ariane

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395 forks

Releases 3

Ariane 4.2 Latest
on 4 Jun 2019

+ 2 releases

Packages

No packages published
Publish your first package

Contributors 62

The CVA6 project team @OpenHW

Three Thales teams:

- Thales Research & Technology (TRT), France
  - Technical project leader
- Thales DIS (INVIA), France
  - Verification leader
- Thales India / Engineering Competence Center (ECC)

Academy & Research contributors:

- ETH Zürich
- U. Bologna (past)
- U. Minho (TBC)

More industrial contributors are welcome

Acknowledgement

FRACTAL

https://fractal-project.eu/

https://www.linkedin.com/company/fractal-european-research-project/

@project_fractal

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Thank you!

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