Agile Design Methodology for Accelerator-Rich Cluster-based RISC-V SoC

Gianluca Bellocchi[1], Alessandro Capotondi[1], Luca Benini[2] and Andrea Marongiu[1]
[1]University of Modena and Reggio Emilia
[2]University of Bologna - ETH Zürich

Introduction

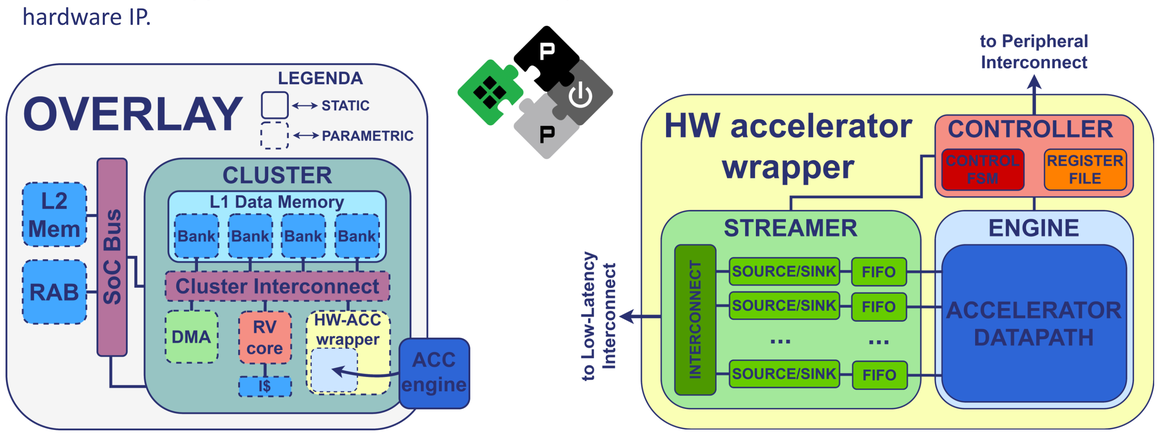
- To enable high performance and energy efficiency, **embedded heterogeneous SoCs** mandate the on-chip integration of general-purpose processors and a plethora of application-specific hardware accelerators in a so-called **accelerator-rich paradigm.**
- The design and testing of the whole system are costly and time-consuming, motivating the need for innovative **automated hardware design flows**.
- Modelling the **accelerator interaction** is a non-straightforward and challenging task.

Motivation

- **System-level design (SLD)** – To streamline the design, integration and evaluation of accelerator-rich systems employing **agile** and **reliable** methodologies.
- **Design space exploration (DSE)** – To explore the design space and find **optimal** HW/SW implementations to meet the wide range of **application-level requirements**.
- **Accelerator design** – Need for more automated **design flows** (e.g. HLS).

Methodology

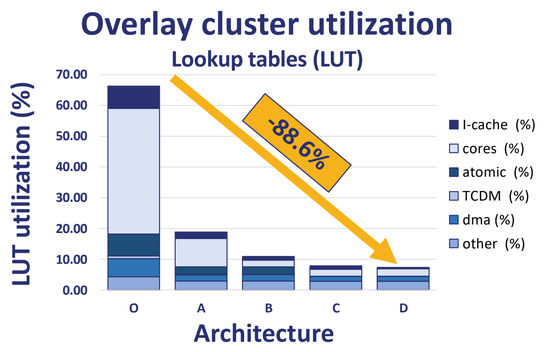
- **FPGA overlay** – Hardware abstraction layer that hides the HW details of the underlying fabric (ASIC, FPGA), thus simplifying system-level design.
- **Accelerator wrapper** – Communication and control protocol for hardware accelerators in the form of a hardware IP.

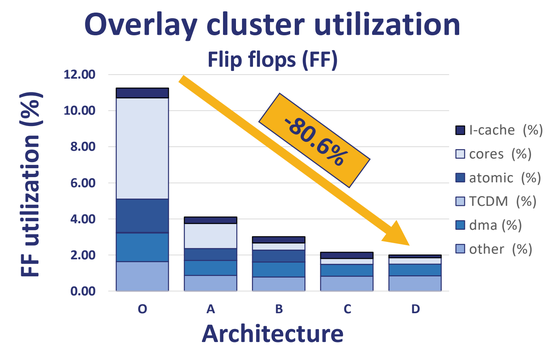


- **Application modelling** – Strong decoupling in designing the wrapper and its accelerator engine (HLS, third-party, etc.).
- **Wrapper generation** – Template-based generation of wrapper resources is fully automated and reliable. Application requirements are specified through a Python interface.
- **System generation** – Generation of a full-custom SoC design to meet the application requirements. Different strategies are to interconnect and orchestrate the accelerator wrappers, increasing the DSE region.
- **Verification and evaluation** – Full support for FPGA deployment and RTL simulation.
- **Prototyping** – Not limited to a specific fabric target: both ASIC and FPGA are good candidates!

Area results

- **Overlay cluster cost –** The less impacting the overlay, the larger the area for acceleration.
  - **Goal** - Resource characterization of a set of (empty) cluster configurations on a Xilinx ZU9EG MPSoC.
  - **Result** - Actual implementation (arch. D) costs: **LUT ≈ 20%, FF ≈ 12%, BRAM ≈ 3.8% and DSP ≈ 0%**.





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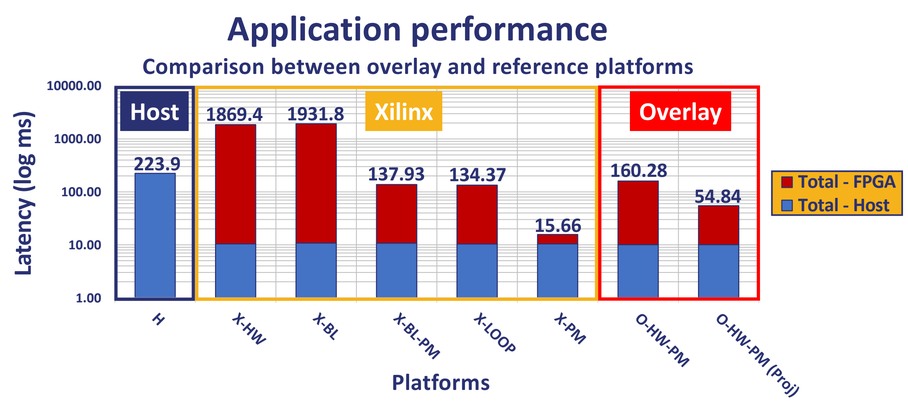
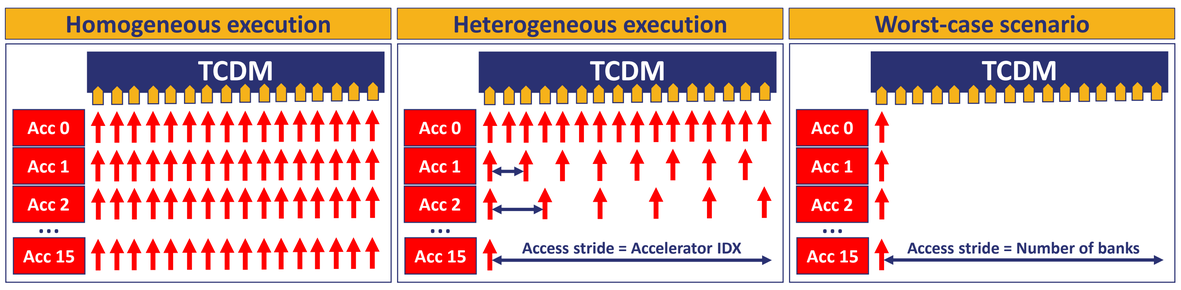
Performance results

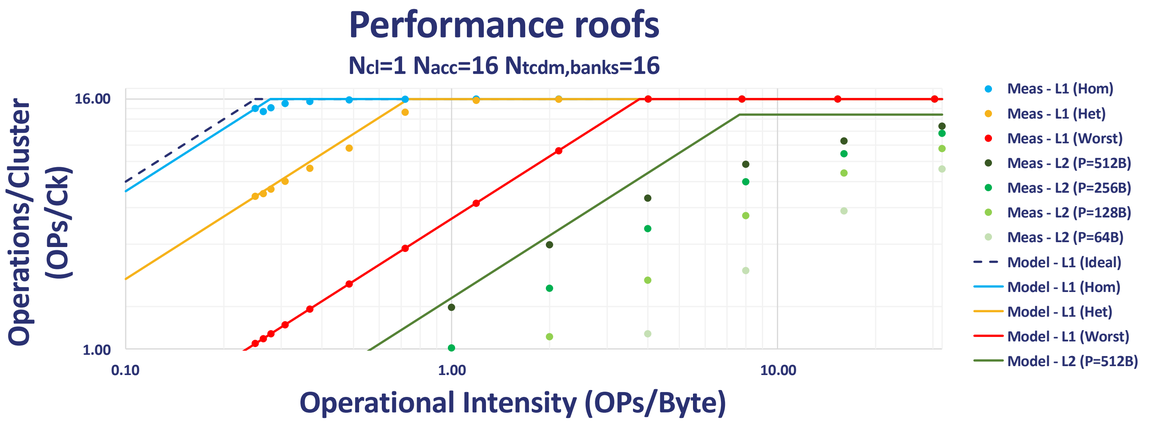
- **Application performance** – How does our solution compare to alternative platforms?
  - **Goal** - Comparison of overlay-based and platform applications on a Xilinx ZU9EG MPSoC.
  - **Algorithm** - HW/SW implementations of a **matrix multiplication (AB)** kernel.
  - **SW reference** - Up to **4.08x** speedup compared to execution on the **host core**.
  - **HW reference** - Comparison to **Xilinx HLS flow** demonstrates **comparable performance** of accelerated applications.



- **Accelerator-rich system evaluation** – Shared memory bandwidth and heterogeneous access patterns are constraining resources in the scalability of highly heterogeneous and dense accelerator-rich systems.
  - **Goal** – Performance characterization using multiple synthetic accelerators, or traffic generators (TGs).
  - **Implemented system** – Instantiation of a system with a single cluster that is enriched with 16 TGs.



  - **Interaction with L1 memory** – Cluster bandwidth reduces by **2.6x** running **heterogeneous loads**, with a **5.2x** improvement over the worst-case scenario.
  - **Interaction with L2 memory** – Another constraint comes from **sequential DMA transfers**. According to the transferred data payload, system bandwidth further reduces from **32.7x** up to **192x** even with homogeneous access patterns.



  - **Multi-cluster scaling** – To solve the bottleneck is necessary to **scale the number of clusters** and distribute the accelerators according to the application requirements.
  - **Design space exploration** – **Automated** search of the optimal working points that fulfill **application requirements** is a goal of our methodology.